IN THE CLAIMS

Amended claims follow:

1. (Currently Amended) A stacked switch using a resilient packet ring protocol comprising:

a plurality of switch modules coupled to one another in a ring topology and each having a plurality of external terminals for interfacing with external devices, where each switch module includes:

[[(a)]]an external interface for communicating with the external terminals, the external interface configured to communicate using a communication protocol; and

[[(b)]]an internal interface for communicating with other switches, the internal interface using a resilient packet ring (RPR) protocol;

wherein statistics associated with a communication of data through at least one of the switch modules are stored;

wherein the statistics are evaluated to generate a link signal representative of desired links/ports to be aggregated; and

wherein a link aggregation port is selectively aggregated to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules.

2. (Currently Amended) The stacked switch of claim 1, wherein each switch module further includes:

[[(c)]]a controller coupled to the external interface and the internal interface and configured to selectively communicate information between the external interface and the internal interface.

3. (Currently Amended) The stacked switch of claim 2, further comprising:

a master management processor coupled to one or more of the switch modules and configured to provide instructions regarding the communication of information

between each switches' external interface and internal interface, and to control data flow; and

a slave management processor coupled to the master management processor through at least one switch and one or more of the switch modules and configured to provide the instructions regarding the communication of information between each switches' external interface and internal interface, and to control the data flow.

4. (Currently Amended) The stacked switch of claim 3 ~~further comprising~~wherein: the master management processor is configured to assign [[the]]a master/slave relationship based on predetermined criteria; and

the slave management processor is configured to become another master management processor if the master management processor fails.

5. (Currently Amended) The stacked switch of claim 3, ~~further comprising~~wherein:

[[a]]the link aggregation port is coupled to one or more switch modules' external terminals and configured to selectively aggregate the information to and from the switch modules.

6. (Currently Amended) The stacked switch of claim 5, further comprising:

a memory configured to store the statistics associated with the communication of data through the at least one switch module;[[and]]

wherein the master management processor is configured to evaluate the statistics in the memory and to generate [[a]]the link signal representative of the desired links/ports to be aggregated~~; and~~

~~wherein the link aggregation port is configured to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules~~.

7. (Currently Amended) The stacked switch of claim 6, wherein:

the master management processor is configured to introduce marker information into the data to ensure that the integrity of the data is reasonably maintained[[.]] when a link aggregation is modified.

8. (Currently Amended) A method of switching data through a stacked switch using a resilient packet ring protocol, the stacked switch having a plurality of modules, where each module includes an external interface for communicating with external terminals and an internal interface for communicating with other switches using a resilient packet ring (RPR) protocol, comprising ~~the steps of~~:

storing statistics associated with [[the]]a communication of data through at least one module in [[the]]a switch; and

evaluating the statistics ~~in the memory and~~ to generate a link signal representative of desired links/ports to be aggregated; and

selectively activating a link aggregation port to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules.

9. (Currently Amended) The method of claim 8, further comprising ~~the step of:~~ [[S]]selectively introducing marker information into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified.

10. (New) The method of claim 8, wherein the statistics are based on port traffic.

11. (New) The method of claim 8, further comprising sending a marker to facilitate handover from a first port to a second port.

12. (New) The method of claim 8, wherein local ports on the switch are aggregated.